Design Review 1, Very Large Scale Engineers, VLSI 4332

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ABSTRACT

This paper provides an overview of our design for embedded static random access memory (SRAM) with a high speed 64 kb cache designed in FreePDK 45nm technology using the Cadence software suite. The design and simulation results presented illustrates to Portable Instruments Company (PICo) the current functionality (read, write, and idle) of one block of our SRAM.

1. INTRODUCTION

Very Large Scale Engineers (VLSE) is seeking to design the most efficient SRAM with a high-speed cache possible for usage in a new mobile communications node. The cache will provide faster speeds only during periods of maximum data transfer, specifically storing data during encryption and compression. The goal is to prove to PICo that our design is the most optimal design and therefore win the contract. The design described in this document along with the schematics, diagrams, simulation results, and layout all provide the necessary proof that our design is currently functional at the bit-cell level. The next steps include optimizing this design with respect to area, delay, and power, with an emphasis placed on delay.

2. DESIGN

2.1 Block Design

We designed one block of the SRAM following the requirements given – e.g. 64 rows by 32 columns. Furthermore, we have built decoders (tree of 1-to-2 decoders) to ultimately be able to read or write an 8 bit word. Figure 1 illustrates our block diagram for the 1MB SRAM. Our reasoning behind this specific design is primarily based on traditional SRAM designs both introduced in classes such as VLSI Design as well as Digital Logic Design, Digital Integrated Circuits, and Computer Architecture. Furthermore, our initial design is similar to those that have been used in previous iterations of this project. Therefore, we are certain our design is a solid choice. The design works through the usage of sense amplifiers and pre-charge components. During a read, the pre-charge will push the respective column's bit lines high and then let it float, which will allow the desired cell to drive its value to the line and then be read through the output block-multiplexer. Throughout this process, a differential voltage sense amplifier will ensure the bit lines maintain the required threshold for a read to occur. We chose a differential voltage sense amplifier introduced in Rabaey because it provided the necessary function for our current design. We will do more research into faster sense amps because sense amps come with every bit cell in the SRAM and must therefore be optimized for speed.

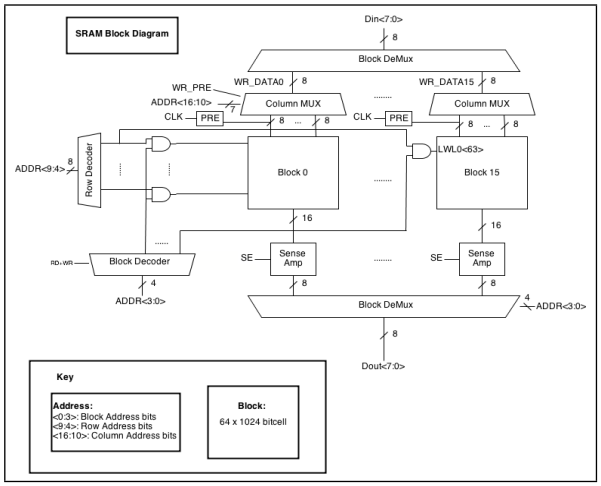


Figure 1: Block Diagram of 1MB SRAM

2.2 Bit Cell Design

The designs and simulations are all centered around a single bit cell for this design review to simply show that one bit cell works. Showing that one bit cell works therefore enables us to wire together many bit cells into a block and with confidence say that the much larger systems will work as well. Therefore, we have focused most of our attention on the lowest level to ensure it exceeds expectations.

The design of the 6T cell is based on two inverters coupled together. Outside of these inverters are word lines (WL) and bit lines (BL). The inverters are connected to the WL through NMOS transistors. Furthermore, the WL is used primarily when reading/writing to a given bit cell. Likewise, the WL is connected to a vertical BL, which is effectively an

access to the word line and therefore stored data. Our sizing decisions are discussed along with the simulation results.

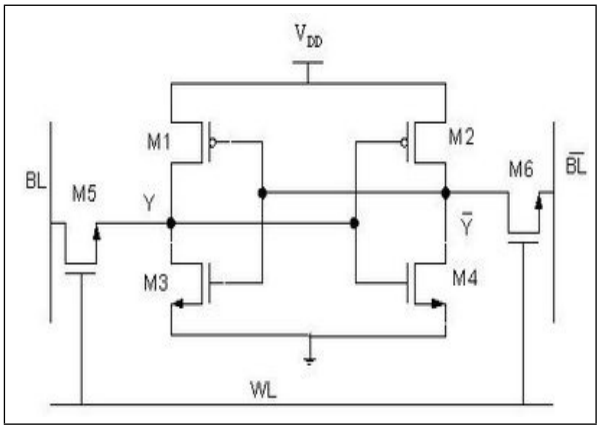


Figure 2: Traditional 6T Bit Cell SRAM Schematic[2]

3. SIMULATION RESULTS

The simulation results illustrate the functionality of our 6T bit cell. All of the inputs and outputs – e.g. WRITE, READ, D/DB, Q/QB, OUT, WL, BL, and PRE (precharge) – behave as expected. Initially, we ran into issues regarding Q and QB, where for some reason, the cell was able to write a perfect 1, but unable to pull down the 1 to a 0 while writing a 0. Interestingly, through debugging the circuit, we found that there was an issue with our NMOS data transistors. After discussing our problem with Professor Calhoun, we realized that our SRAM was behaving correctly; however, the SRAM was not performing accurately. The data NMOS transistors attempted to pull down the value, but the cell ratio and widths needed to be adjusted because the NMOS was too weak. We adjusted our ratios and changed our values to micron widths, as opposed to nanometer widths, for the time being, due in part to the cell ratio discussion in class. Lastly, there are odd pulse widths in the write simulation (in the attached document), that we believe may also be attributed to sizing. All in all, our simulations show basic functionality, but we will need to refine before we optimize.

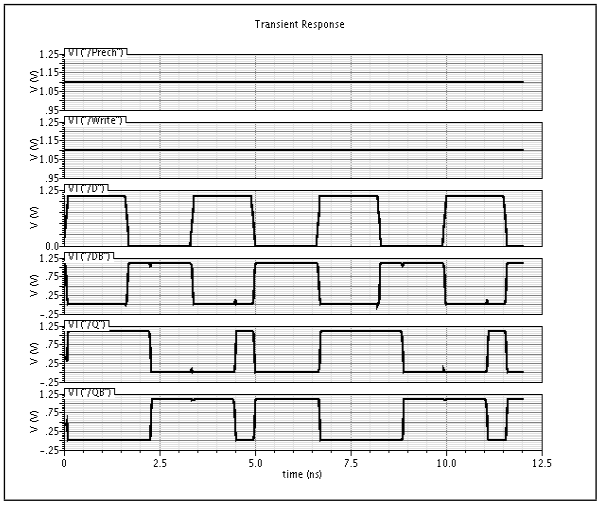


Figure 3: Write Simulation Results for 6T Bit Cell

4. NEXT STEPS

The following is a list of completed tasks prior to the formal submission of our design proposal. The documentation of these tasks and any results or schematics can be found at the end of this document.

- ✓ Block Diagram showing conceptual arrangement of major SRAM components
- ✓ Gate Level Schematic from Cadence of one block of the array
- ✓ Timing Diagram for the Memory specifically showing read and write operations
- ✓ Functional Bit Cell Layout
- ✓ Simulation Results

Following the design proposal, the following tasks will be completed:

- Perform rigorous process corner check and ensure solid data integrity
- Optimize SRAM for high speed caching usage
- Revise Memory Block Diagram with registers as well as more specific sizings and details
- Simulate aspects of entire memory array wired together – e.g. Decoders, Sense Amp, Blocks, etc.

5. ACKNOWLEDGMENTS

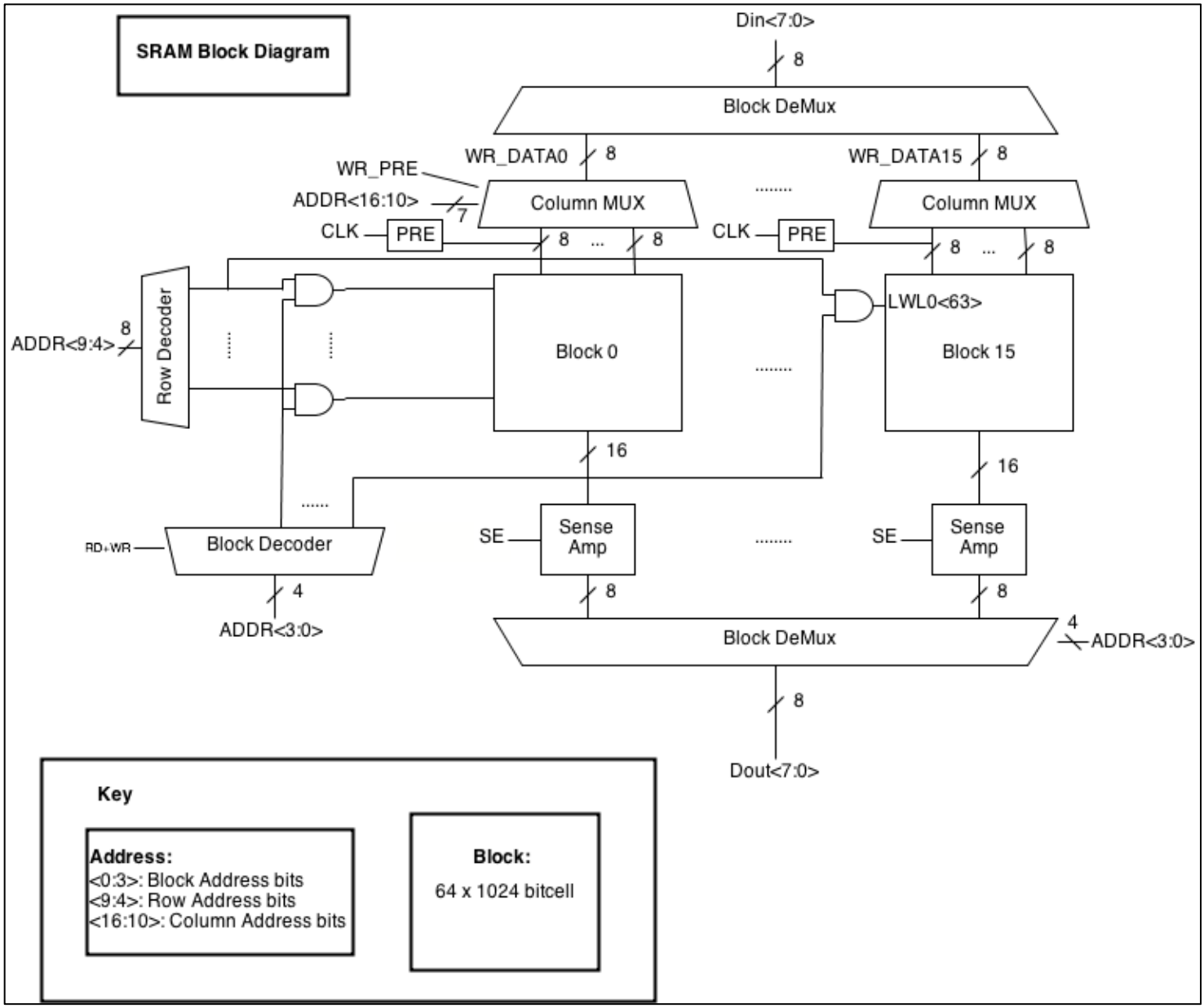
We would like to thank Professor Benton Calhoun, Professor Aatmesh Shrivastava, and Divya Akella for their guidance and support throughout this first design review.

6. REFERENCES

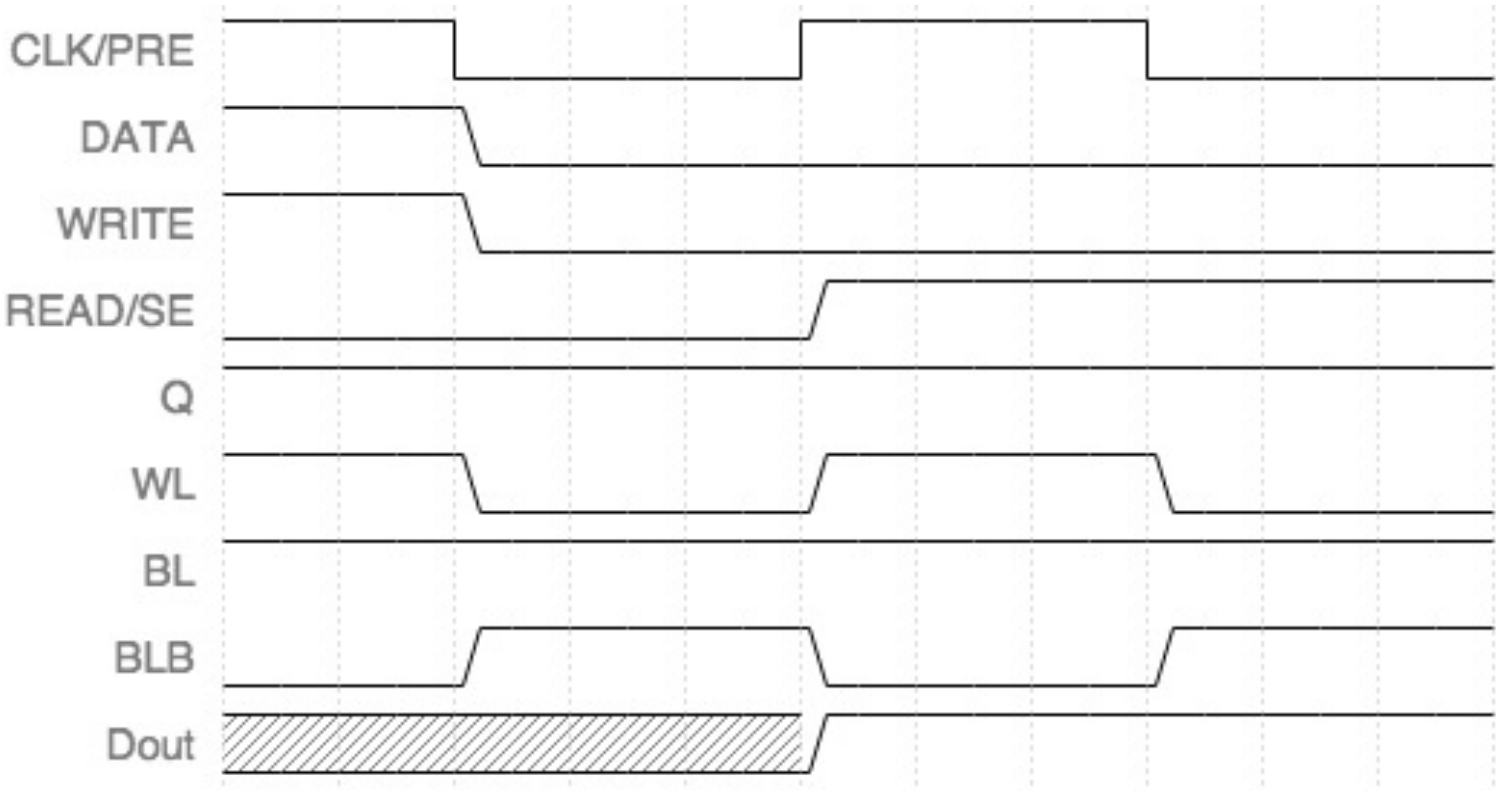
[1] Rabaey, J., Chandrakasan A., Nikolic, B., *Digital Integrated Circuits (2^{nd} Edition)*, (Dec 24, 2002)

[2] "SRAM Cell Design." *ASIC-System on Chip-VLSI Design.* N.p., n.d. Web. 08 Oct. 2013.

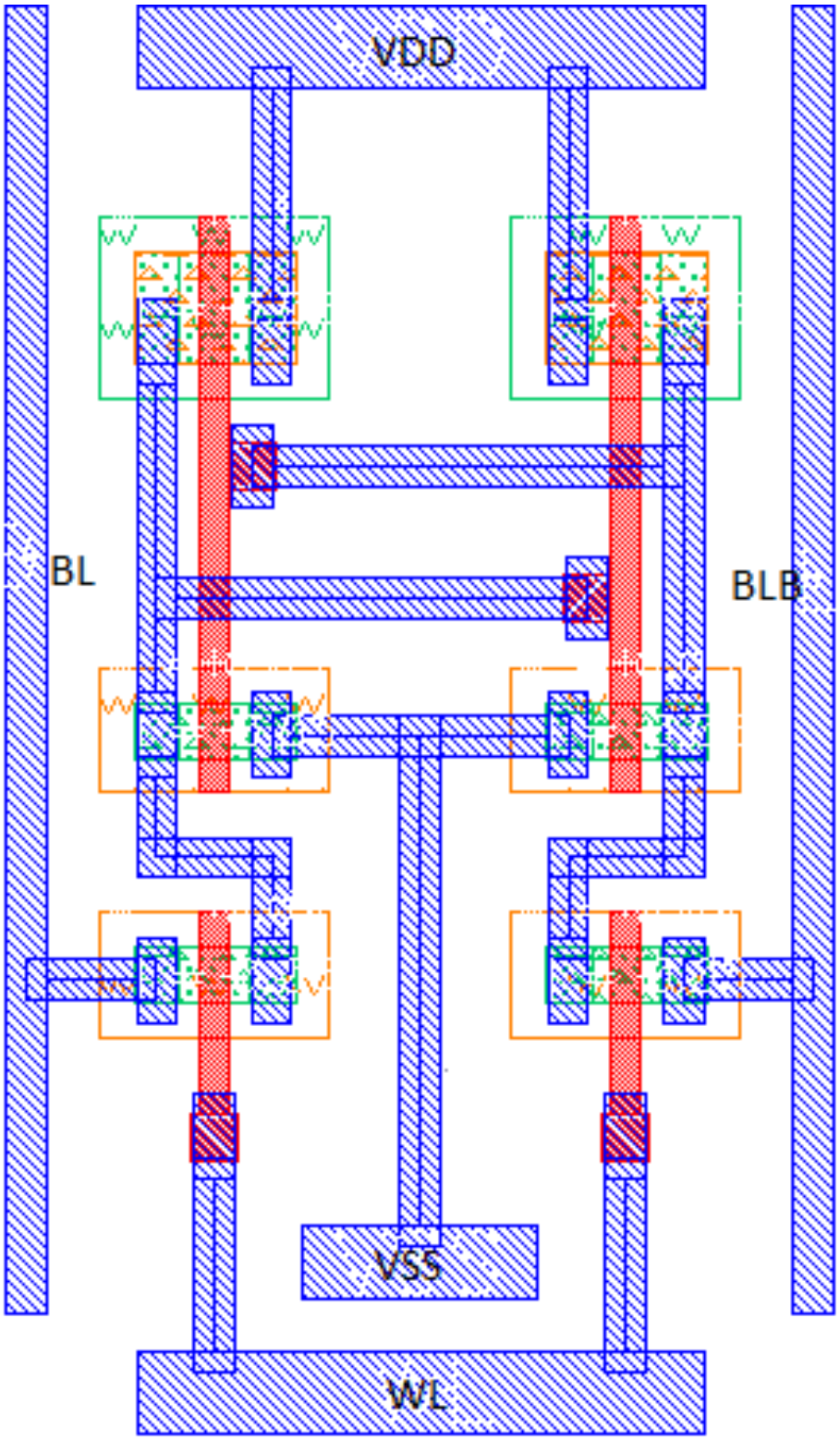
Block Diagram



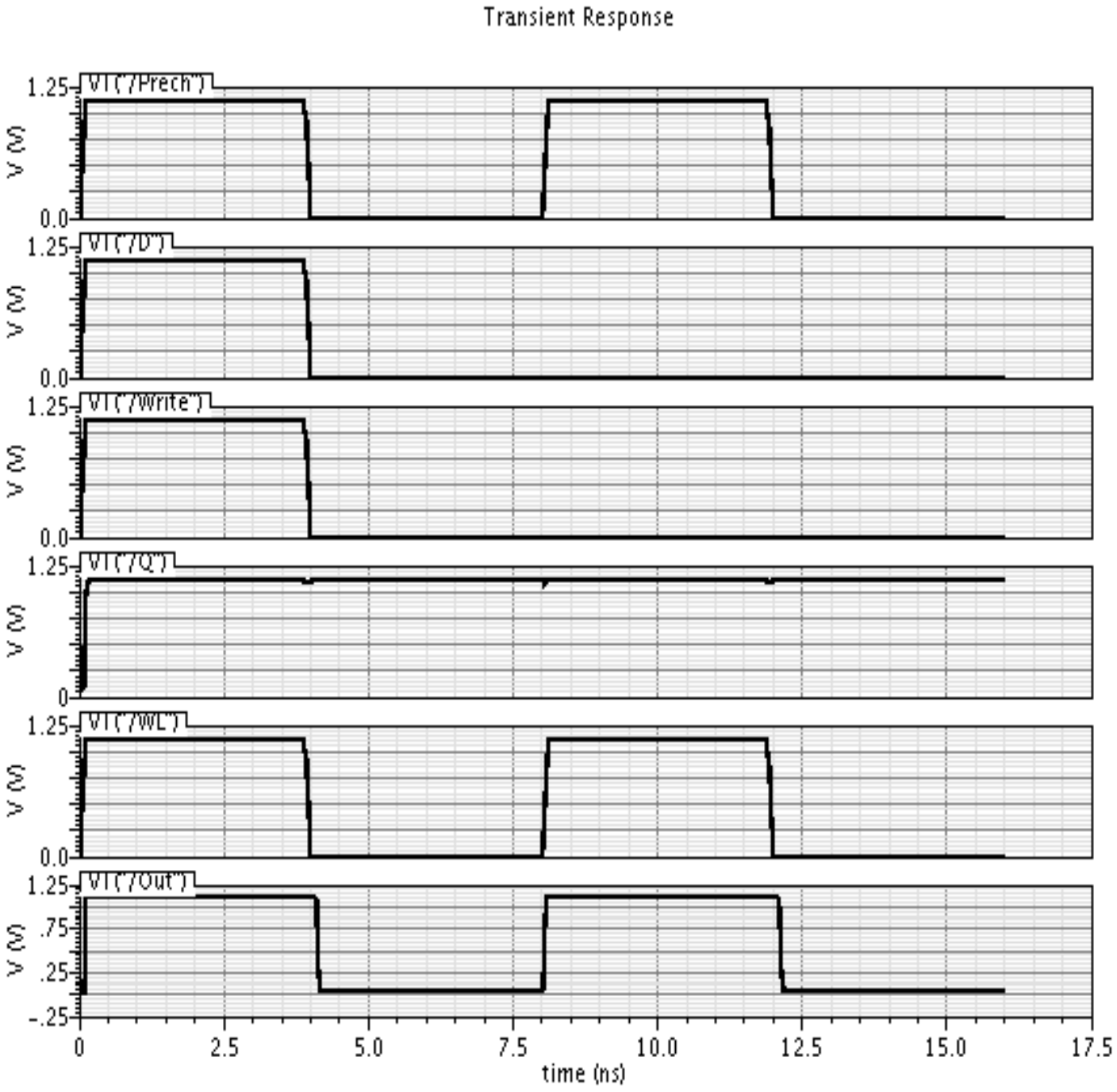
Timing Diagram (Write 1, then Read)



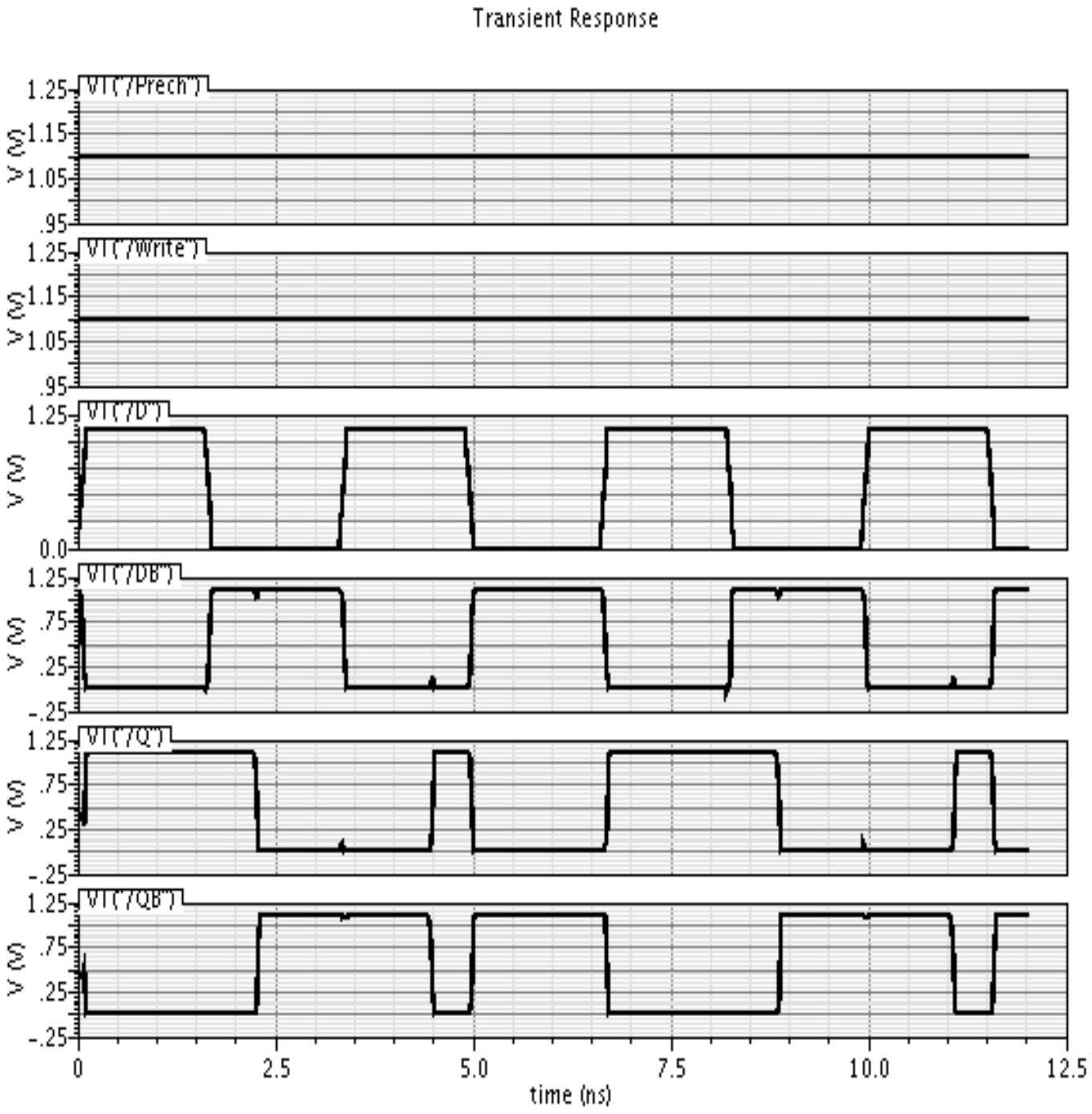
6T Bit Cell Layout



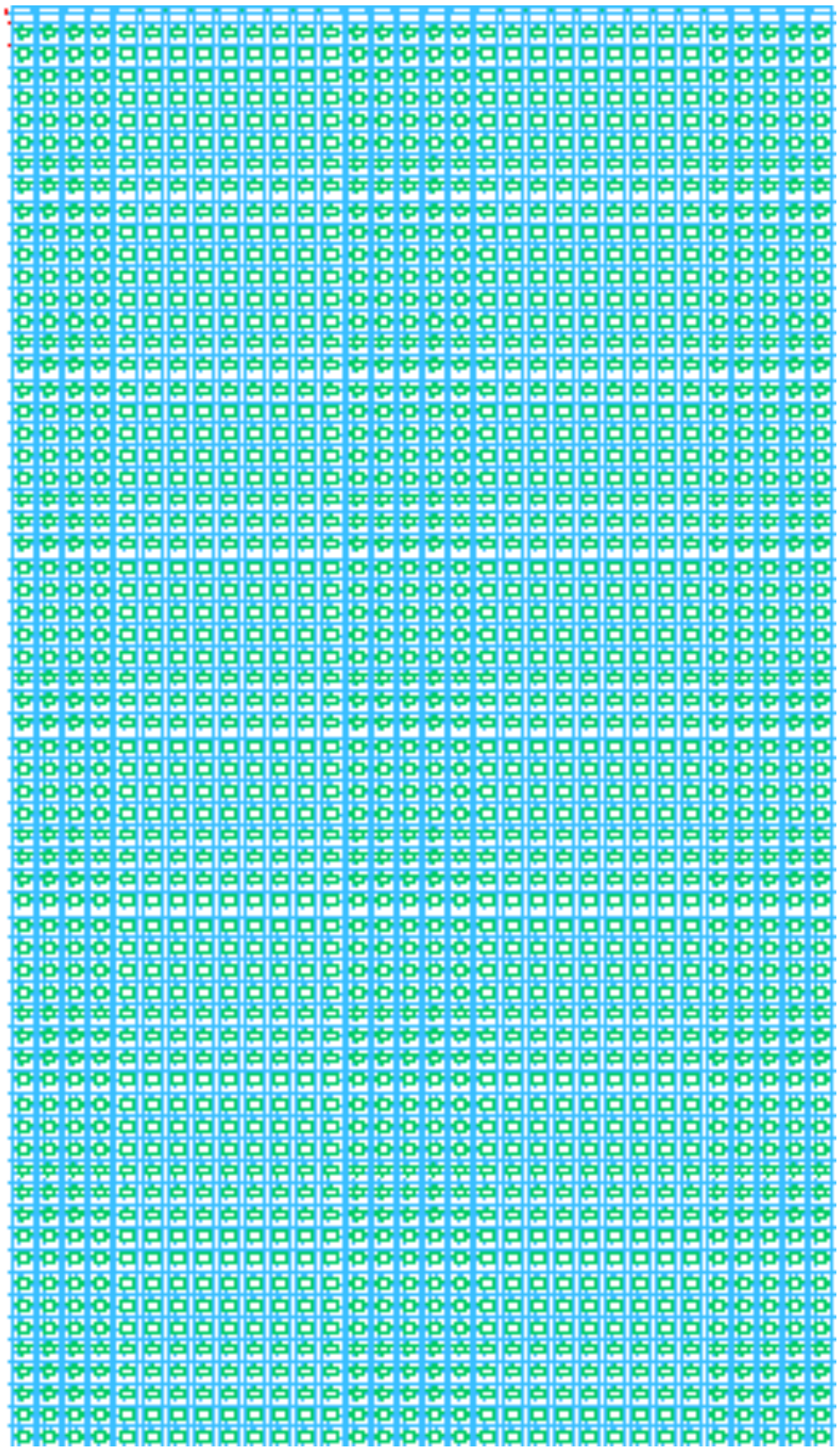
6T Bit Cell Write and Read Simulation



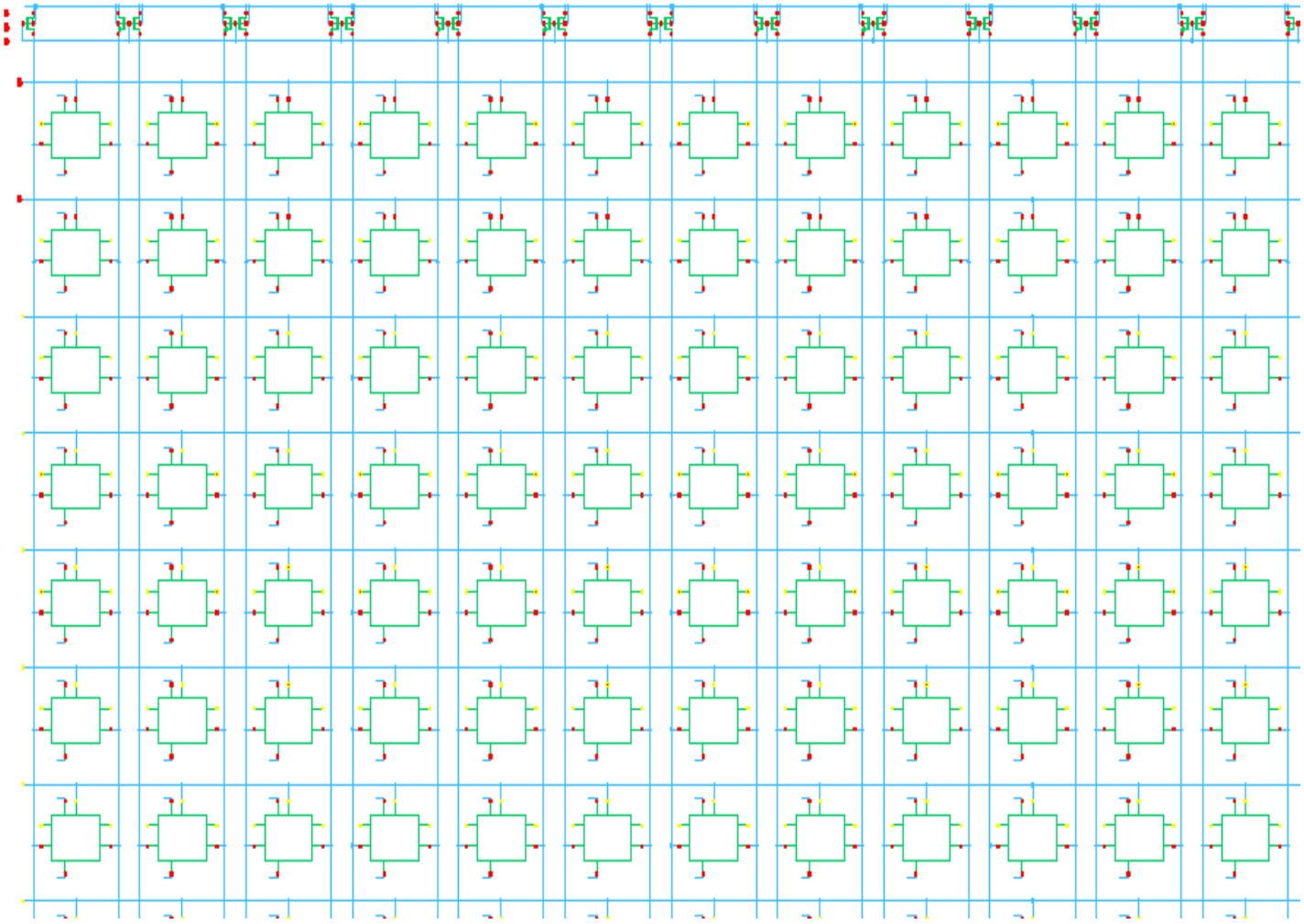
6T Bit Cell Write Simulation



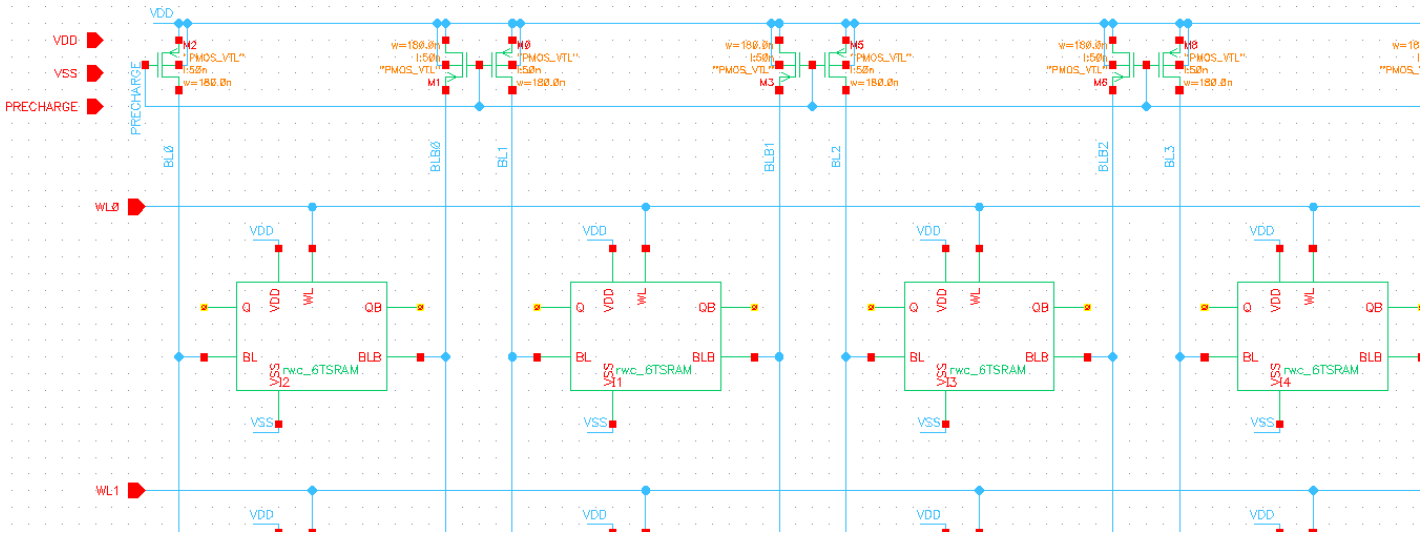
Array Block Cadence Schematic (Overview)



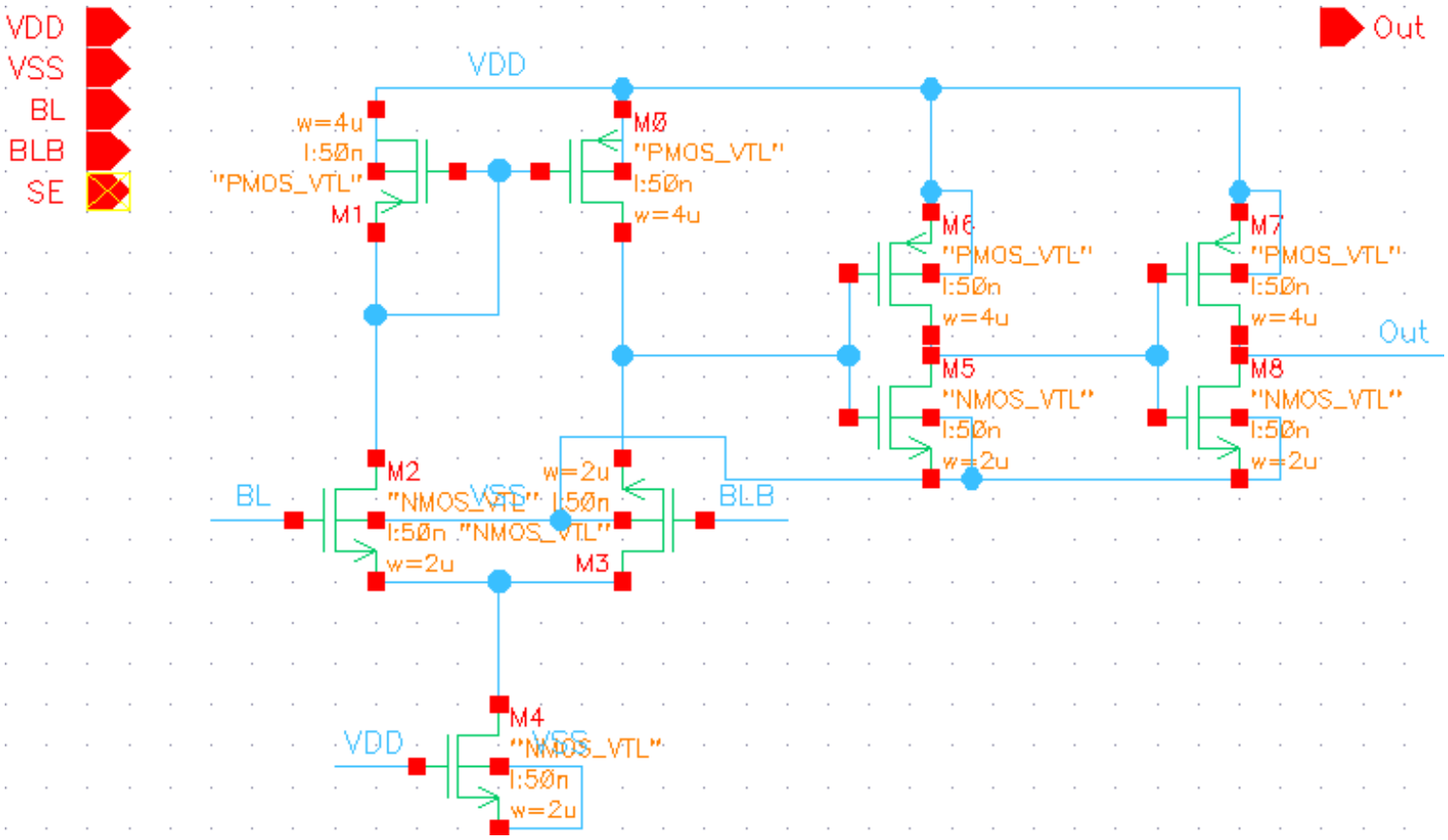
Array Block Cadence Schematic (Intermediate)



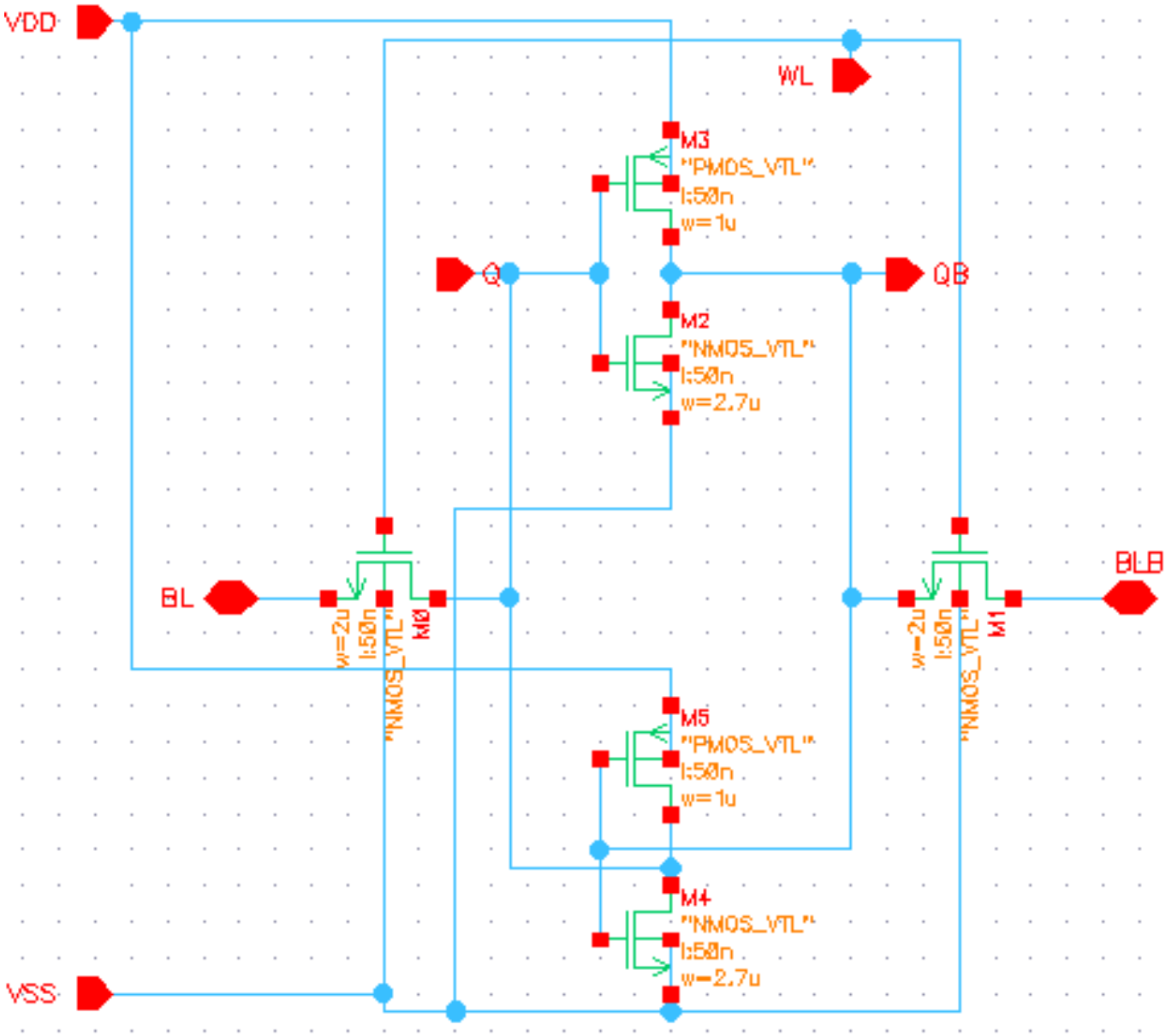
Array Block Cadence Schematic (Closeup)



Sense Amplifier Schematic



6T Bit Cell Schematic



6T Bit Cell Test Bench